IN THE CLAIMS:

Please cancel claims 19-25 without prejudice or disclaimer as to the subject matter recited therein. Applicants reserve the right to file one or more divisional applications at a later date capturing the subject matter recited in claims 19-25 canceled herein.

1. (Original) A bus bridge circuit, wherein the bus bridge circuit is adapted for coupling to a first bus comprising n address lines, and wherein *n* is and integer and *n* >= 2, and wherein the bus bridge comprises:

audio logic configured to access digital audio data and to produce an *n*-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit; and

wherein when the audio logic is accessing the digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the *n*-1 bit address to produce an *n*-bit address, wherein the additional address bit forms a most significant bit of the *n*-bit address, and (ii) drive the *n* bit address upon the *n* address lines of the bus.

2. (Original) The bus bridge circuit as recited in claim 1, wherein the addressable register has an address, and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register.

3. (Original) The bus bridge circuit as recited in claim 1, wherein the *n* address lines of the first bus define an address space of the first bus, and wherein a bit stored in the bit position of the addressable register via a write operation determines whether the *n*-bit

address resides in a lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

4. (Original) The bus bridge circuit as recited in claim 1, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines.

5. (Original) The bus bridge circuit as recited in claim 1, wherein the bus bridge circuit is further adapted for coupling to a second bus, and wherein the bus bridge circuit is configured to translate signals between the first and second bus.

6. (Original) The bus bridge circuit as recited in claim 5, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines, and wherein the second bus is an industry standard architecture (ISA) bus.

7. (Original) The bus bridge circuit as recited in claim 1, wherein the audio logic is adapted for coupling to a speaker, and wherein the audio logic is configured to receive digital audio data, to transform the digital audio data to an analog signal, and to provide the analog signal to the speaker.

8. (Original) The bus bridge circuit as recited in claim 1, wherein the audio logic is adapted for coupling to a microphone, and wherein the audio logic is configured to receive an analog signal from the microphone, to transform the analog signal to digital audio data representing the analog signal, and to provide the digital audio data.

9. (Original) A computer system comprising:

a first bus, wherein the first bus comprises *n* address lines, and wherein *n* is and integer and $n >= 2$;

a bus bridge circuit coupled to the first bus, wherein the bus bridge circuit comprises:

audio logic configured to access digital audio data and to produce an n-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit; and

wherein when the audio logic is accessing the digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the n-1 bit address to produce an n-bit address, wherein the additional address bit forms a most significant bit of the n-bit address, and (ii) drive the n bit address upon the n address lines of the bus.

10. (Original) The computer system as recited in claim 9, wherein the addressable register has an address, and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register.

11. (Original) The computer system as recited in claim 9, wherein the n address lines of the first bus define an address space of the first bus, and wherein a bit stored in the bit position of the addressable register via a write operation determines whether the n-bit address resides in a lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

12. (Original) The computer system as recited in claim 9, wherein the first bus is a peripheral component interconnect (PCI) bus having n multiplexed address/data lines.

13. (Original) The computer system as recited in claim 9, wherein the bus bridge circuit is further adapted for coupling to a second bus, and wherein the bus bridge circuit is configured to translate signals between the first and second bus.

14. (Original) The bus bridge circuit as recited in claim 5, wherein the first bus is a peripheral component interconnect (PCI) bus having *n* multiplexed address/data lines, and wherein the second bus is an industry standard architecture (ISA) bus.

15. (Original) The computer system as recited in claim 9, wherein the audio logic is adapted for coupling to a speaker, and wherein the audio logic is configured to receive digital audio data, to transform the digital audio data to an analog signal, and to provide the analog signal to the speaker.

16. (Original) The computer system as recited in claim 9, wherein the audio logic is adapted for coupling to a microphone, and wherein the audio logic is configured to receive an analog signal from the microphone, to transform the analog signal to digital audio data representing the analog signal, and to provide the digital audio data.

17. (Original) A computer system comprising:

a first bus comprising *n* address lines, and wherein *n* is and integer and $n >= 2$;

a second bus;

a bus bridge circuit coupled between the first bus and the second bus, wherein the bus bridge circuit is configured to translate signals between the first bus and the second bus;

wherein the bus bridge circuit comprises:

audio logic configured to access digital audio data and to produce an *n*-1 bit address when accessing the digital audio data; and

an addressable register comprising a bit position for storing an additional address bit, wherein the addressable register has an address, and wherein a value

may be stored in the addressable register via a write operation specifying the address of the addressable register; and

wherein when the audio logic is accessing the digital audio data, the bus bridge circuit is configured to: (i) concatenate the additional address bit with the n-1 bit address to produce an n-bit address, wherein the additional address bit forms a most significant bit of the n-bit address, and (ii) drive the n bit address upon the n address lines of the bus.

18. (Original) The computer system as recited in claim 17, wherein the n address lines of the first bus define an address space of the first bus, and wherein a bit stored in the bit position of the addressable register via a write operation determines whether the n-bit address resides in a lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

19-25. (Cancelled)